IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANTS' APPEAL BRIEF TRANSMITTAL LETTER

APPLICANT:	Schwalke, et al.	DOCKET NO:	P99,2666
SERIAL NO.:	09/462,994	ART UNIT:	2823
FILED:	January 14, 2000	EXAMINER:	B. Kebede

TITLE: Integrated Circuit Arrangement and Method for the Manufacture Thereof

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Appellants are submitting herewith, in triplicate, Appellants' Brief Under 37 C.F.R. §1.192 in support of the Notice of Appeal filed May 10, 2004.

Appellants have enclosed a check for the $330.00 due as required by 37 C.F.R. §1.17(c). The Commissioner is hereby authorized to charge any additional fee that may be required to deposit account No. 50-1519. A duplicate copy of this sheet is enclosed.

Submitted by,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on July 13, 2004.

Mark Bergner

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

APPELLANTS' MAIN BRIEF ON APPEAL

APPLICANT:	Schwalke, et al.	DOCKET NO:	P99,2666
SERIAL NO.:	09/462,994	ART UNIT:	2823
FILED:	January 14, 2000	EXAMINER:	B. Kebede

TITLE Integrated Circuit Arrangement and Method for the Manufacture Thereof

Mail Stop Appeal Brief-Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. §1.192, Appellants submit this Brief in support of the appeal of the above-referenced application, in triplicate, in support of the patentability of claims 11-24 (claims 11, 12, and 15-24, as currently amended) finally rejected in the Office Action, dated November 14, 2003 ("OA"). A telephone interview with the Examiner conducted on April 29, 2004 did not result in agreement. A copy of the claims on appeal is attached as Appendix A. A Notice of Appeal was filed on May 13, 2004.

REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee, Infineon Technologies AG, a German corporation, by virtue of an assignment executed December 9, 1999 and recorded on January 14, 2000 at reel/frame: 010593 / 0439.

RELATED APPEALS AND INTERFERENCES:

There are no related appeals and no related interferences known to Appellants, Appellants' Assignee, or Appellants' legal representative.

STATUS OF CLAIMS:

Claims 11-24 were rejected in the Final Office Action. As currently amended, claims 11, 12, and 15-24 are on appeal. The claims were rejected in the Final Office Action as follows:

Claims / Section	35 U.S.C. Sec.	References / Notes
11, 15, 16, 18 & 21-24	§102(b) Anticipation	• Hirakawa, et al. (U.S. Patent No. 4,590,508).
11 & 13-21	§102(e) Anticipation	• Shimomura, et al. (U.S. Patent No. 5,736,421).
12	§103(a) Obviousness	• Shimomura, et al. (U.S. Patent No. 5,736,421); • Uehara, et al. (U.S. Patent No. 5,698,902).
22, 24	§132	• New matter entered
22, 24	§112, ¶1	• Lack of written description

STATUS OF AMENDMENTS:

Appellants have amended claim 11 to include the limitations of claims 13 and 14 for the purposes of this appeal, and respectfully request entry of this amendment.

SUMMARY OF THE INVENTION:

The planarization of semiconductor layers is significant in the manufacture of semiconductor devices. In these devices, useful structures having a circuit oriented function, such as terminal electrodes, gate electrodes or interconnects, are manufactured in planes by structuring a previously

produced layer. Insulation layers are provided between successive planes. These insulation layers are planarized by polishing and/or etching. 1/3-11.

When the useful structures and the filler structures are composed of conductive material, then the filler structures can become charged during operation of the device. In order to avoid this, it is known to apply the filler structures to a fixed potential, by contacting them via a specific wiring that is arranged in a metallization plane arranged above the useful and filler structures. However, this additional wiring and the contacts between the additional wiring and the filler structures makes the production of the layout more difficult. 1/12-28.The invention provides an integrated circuit arrangement that can be manufactured with high planarity, whereby a charging of electrically conductive filler structures is avoided and for which the layout can be produced with reduced outlay. An appertaining method is further provided. 2/1-8.

According to embodiments of the invention, a doped region is provided in a semiconductor substrate in the integrated circuit arrangement. A plane with conductive useful structures and at least one conductive filler structure is arranged at the surface of the semiconductor substrate. This conductive filler structure is conductively connected to the doped region., such as the substrate body and/or a doped well in which components are arranged; these are already charged with a fixed supply voltage in integrated circuit arrangements during operation. 2/9-18.

The connection to the conductive filler structure assures that the

conductive filler structure also lies at this potential. Since the doped well or the substrate body are already connected to fixed potential, the additional wiring that is only provided for the purpose of connecting the filler structures can be omitted in the inventive integrated circuit arrangement, simplifying the layout and permitting production by automatic layout generation. The position of the filler structure can be determined in a program-controlled manner. 2/18-24.

The electrical connection of the conductive filler structure to the doped region may ensue by way of a via hole and a contact. The via hole overlaps the conductive filler structure and the doped region so that the surface of the conductive filler structure and of the doped region are in communication with the contact. The via hole and the contact are preferably produced simultaneously with via holes and contacts to conductive useful structures. No additional process steps are therefore required for this purpose. Since only extremely slight current (chargings, capacitative shift currents, etc.) need be eliminated, an overlapping contact is not compulsory. In principle, the side wall contact surface already suffices. Other high-impedance eliminations via components are suitable for this purpose. 2/25-3/6.

It is also possible to arrange a metallization level above the plane in which the conductive filler structure is arranged and to connect the filler structure to the metallization level to which the filler structure is connected via the further contact that lies at the same potential as the doped region during operation. The contact and the further contact then form an additional

integrated contact for the doped region. The plane in which the conductive filler structure is arranged can be either a gate plane that is arranged in the proximity of the surface of the semiconductor substrate or a metallization plane that is arranged above the gate plane and/or further metallization planes. 3/12-21.

For manufacturing the integrated circuit arrangement, a doped region is formed in the semiconductor substrate. The plane with conductive useful structures and at least one conductive filler structure is formed on the semiconductor substrate by application and structuring of a conductive layer. An insulation structure is generated that surrounds the conductive useful structures and the conductive filler structure and covers them. Since the conductive useful structures and the conductive filler structure are formed of the conductive layer, they exhibit essentially the same height. The connection between the doped region and the conductive filler structure may be produced by opening a via hole that overlaps the conductive filler structure and the doped region, and by formation of a contact. 3/22-4/2

The connection of the conductive filler structure to the doped region can be alternatively undertaken via a local wiring level. What is referred to as local wiring level is an electrically conductive connection that is effective in the lateral environment. When the plane in which the conductive filler structure is arranged is the gate plane, the conductive useful structures contain gate electrodes. The gate electrodes can be formed either by structuring a conductive layer, from which the conductive filler structure is then formed, or

by structuring a plurality of sub-layers. 4/7-4/15.

Part of the doped region that is overlapped by the via hole for connection to the conductive filler structure may be separated from parts of the doped region in which active elements of the circuit arrangement are arranged, being separated therefrom by an insulation structure, for example, a trench filled with insulating material. In this case, the doped region extends more deeply into the substrate than the insulation structure, avoiding shorts between active elements and the contact. 4/16-4/22.

ISSUES:

The issues on appeal are as follows:

1. Whether claim 11, as amended to include the limitations of claim 14 (which depended from claim 13), is anticipated under 35 U.S.C. §102 by Shimomura, et al. (U.S. Patent No. 5,736,421).

2. Whether claim 18 is anticipated under 35 U.S.C. §102 by Shimomura, et al. (U.S. Patent No. 5,736,421).

3. Whether claim 18 is anticipated under 35 U.S.C. §102 by Hirakawa, et al. (U.S. Patent No. 4,590,508).

4. Whether the addition of claims 22 and 24 constitute the introduction of new matter according to 35 U.S.C. §132.

5. Whether the addition of claims 22 and 24 lack a written description according to 35 U.S.C. §112, ¶1.

GROUPING OF CLAIMS:

The claims on appeal include two independent claims (claim 11 and 18) and twelve dependent claims (11, 12 and 15-24).

Group 1: claims 11, 12, 15, 16, 17, 21 & 22

The primary basis of dispute for the rejection of the apparatus claims revolves around independent claim 11 (as amended). Appellants group dependent claims 12, 15, 16, 17, 21 & 22 in the group with claim 11. These claims stand or fall together.

Group 2: claims 18-20, 23 & 24

Appellants believe that claim 18 and respective claims 19, 20, 23 and 24 depending therefrom are separately patentable, and thus places them in a second group for appeal. These claims are separately patentable since they are directed to a method of manufacturing, and since the Examiner has used a separate basis for rejection of these claims in the Final Office Action. These claims stand or fall together, but do not stand or fall with the claims in Group 1.

ARGUMENTS:

ARGUMENT 1–Anticipation of Claim 11 by Shimomura

Examiner's Position: Claim 11 (formerly 14) is anticipated by Shimomura because Shimomura teaches all of the elements of claim 11, including a conductive filler structure having no circuit-oriented function that exhibits essentially the same height as the conductive useful structures and is conductively connected to the doped region.

In the OA on pages 5-6, the Examiner states:

> Re claim 11, Shimomura et al. disclose an integrated circuit arrangement having at least one doped region (106) is provided in a semiconductor substrate (101); a plane arranged on a surface of the semiconductor substrate (101) having a number of conductive useful structures (113) and at least one conductive filler structure (112) (i.e., a dummy gate or resistor) which exhibits essentially the same height, said conductive filler structure having no circuit-oriented function; and the conductive filler structure (112) is conductively connected to the doped region (106) (see Fig. 1).
>
> Re claim 13, as applied to claim 11 above, Shimomura et al. disclose all the claimed limitation including the limitation a contact (not labeled) connecting the conductive filler structure (112) to the doped region (106) via a via hole (not labeled) (see Fig. 1).
>
> Re claim 14, as applied to claim 13 above, Shimomura et al. disclose all the claimed limitation including the limitation wherein said through hole (not labeled) overlaps said conductive filler structure (112) and said doped region (106) exposing surface of the said conductive filler structure (112) and said a surface of said doped region (106), said contact (not labeled) being in communication with said conductive filler structure (112) and said surface of the doped region (106) (see Fig. 1).

In the Examiner's Response to Arguments Section, on pages 15-16, the Examiner states:

> In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly, as stated above. The Examiner respectfully submits that Shimomura et al. '421 disclose all the claimed limitation as applied herein above. In addition, Shimomura et al. also disclose including the limitation one conductive filler structure which exhibits essentially the same height, said conductive filler structure having no circuit-oriented function.
>
> Furthermore, the rejected claim, i.e... claim 11, does not claim that "the conductive useful structures and the conductive filler structure are both formed by applying and structuring a conductive layer which means applying and structuring one and the same conductive layer" as applicants argued. Therefore, applicants' argument that the references fail to show certain features of applicant's invention, it is noted that the features

> upon which applicant relies (i.e., the conductive useful structures and the conductive filler structure are both formed by applying and structuring a conductive layer which means applying and structuring one and the same conductive layer) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellants' Position: Shimomura fails to disclose the element of claim 11 that the filler structure and useful structures have essentially the same height and other elements of the claim.

Claim 1, as one of its elements, requires that the arrangement has a plane arranged on a surface of the semiconductor substrate having a number of conductive useful structures and at least one conductive filler structure which exhibits essentially the same height.

The phrase "which exhibits essentially the same height" is clearly illustrated by referring to Fig. 4 of the application and the appertaining description in the specification at 6/26-29:

> Subsequently, a planarizing insulation layer 11 is formed, this being ground back to such an extent by chemical-mechanical polishing that it terminates in height with the conductive useful structure 71 and the conductive filler structures 72 (see Figure 4).

Figure 4 clearly shows the conductive useful structure 71 and the conductive filler structure 72 along with the planarizing insulation layer 11 at the same height.

The Examiner asserts, without any basis, that Shimomura discloses, "a number of conductive useful structures (113) and at least one conductive filler structure (112) which exhibits essentially the same height." Elements 112 and 113 of Shimomura are clearly not related to a plane arranged on a surface of

the substrate, and do not exhibit "essentially the same height". It appears as though the Examiner is making a reference to the thickness of the respective elements—even so, there is no disclosure for elements 112 and 113 as having the same height. A careful measurement of these elements in Figure 1 of Shimomura (likely not to scale, but this is unimportant for the purposes of disclosure), reveals that element 112 in the figure has a thickness of 0.17", whereas element 113 in the figure has a thickness of 0.12"—even by the use of this measurement, these elements of Shimomura are not "essentially the same height".

Second, element 112 of Shimomura is not a "conductive filler structure", as it does not serve to *fill* any aspect of the plane arranged on the surface of the semiconductor substrate having the useful and filler structures. Element 112 of Shimomura extends and protrudes above an elevated upper surface of oxide 105, and thus does not serve a "filling" role as required by the claim language.

Finally, element 112 of Shimomura is a resistor, and not a "dummy gate structure" as indicated by the Examiner. The key characteristic of a "resistor" is its limited ability to transport electrical charges and it is utilized as such in Shimomura. The *conductive* filler structure (exemplified by a conductive metal line) does not possess such a limited ability as the resistor.

Regarding the elements added by the addition of claims 13 and 14, the Examiner stated, on page 6 of the OA that Shimomura discloses all claimed limitations, Including the limitation a contact (not labeled) connecting the

conductive filler structure (112) to the doped region (106) via a via hole (not labeled) (see Fig. 1)". Fig. 1 of Shimomura does not show a through hole that overlaps both the conductive filler structure (112) and the doped region (106) with the elements equated as the Examiner has done. No overlap is present in Shimomura.

The Examiner indicated that Office personnel are to give claims their broadest reasonable interpretation in light of the supporting disclosure, however, the Examiner, in doing so, is not permitted to ignore features that are clearly cited as elements of the claims.

ARGUMENT 2–Anticipation of Claim 18 by Shimomura

Examiner's Position: Claim 18 is anticipated by Shimomura because Shimomura teaches all of the elements of claim 18, including forming a plane on a surface of said semiconductor substrate by applying and structuring a conductive layer, said plane having a number of conductive useful structures and at least one conductive filler structure.

In the OA on page 7, the Examiner states:

> Re claim 18, Shimomura et al. disclose a method for manufacturing an integrated circuit arrangement comprising: forming a doped region (106) in a semiconductor substrate (101); forming a plane (not labeled) on a surface of the semiconductor substrate (101) by applying a structuring a conductive useful structures (113) and at least one conductive filler structure (112) producing an insulation layer (106) surrounding and covering the conductive useful structures (113) and the conductive filler structure (112); and producing a conductive connection between the conductive filler structure (112) and the doped region (106) (see Fig. 6-9(e)).

In the Examiner's Response to Arguments Section, on page 15, the Examiner states:

> In response to the applicant's argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly [sic], as stated above. The Examiner respectfully submits that Shimomura et al. '421 disclose all the claimed limitations as applied above.

Appellants' Position: Shimomura fails to disclose the element of claim 18 of forming a plane on a surface of said semiconductor substrate by applying and structuring a conductive layer, said plane having a number of conductive useful structures and at least one conductive filler structure.

Appellants do not see a Figure 9(e) referred to by the Examiner in Shimomura. Figs. 7 & 8 are to a graph and block diagram respectively and Fig. 6 does not contain the reference characters discussed by the Examiner. Appellants therefore presume that the Examiner is referring to Fig. 1.

With the elements as equated by the Examiner, Appellants do not see how Shimomura forms a plane on a surface of the semiconductor by applying and structuring a conductive layer, said plane having a number of conductive useful structures 113 and conductive filler structures 112. Appellants are unable to find a plane in Shimomura having elements 112 and 113.

Argument 3—Anticipation of Claim 18 by Hirakawa

Examiner's Position: Each of the elements of claim 18 are disclosed by Hirakawa.

In the Office Action, on pages 4-5, the Examiner states:

> Re claims 18, 23, and 24, Hirakawa et al. disclose a method for manufacturing an integrated circuit arrangement comprising: forming a doped region (103-7) in a semiconductor substrate (201); forming a plane (not labeled) on a surface of the semiconductor substrate (201) by applying a structuring a conductive useful structures (104-1 104-2) and at least one conductive filler structure (not labeled) producing an insulation layer (207) surrounding and covering the conductive useful structures (104-1 104-2) and the conductive filler structure (not labeled); and producing a conductive connection between the

conductive filler structure (not labeled) and the doped region (103-7); including the limitation wherein conductive useful structures and the conductive filler structure exhibit essentially the same height and the conductive filler structure has not circuit orientated function and have uniform geometrical occupation (see Figs. 1-10).

In the Examiner's Response to Arguments section on pages 11-14, the Examiner states:

> In response to the applicants argument, the Examiner respectfully submits that such an argument is not commensurate with the scope of the claims, in particularly [sic], as stated above.
>
> The Examiner's remaining comments are solely directed to elements of claim 11.

Appellants' Position: Hirakawa fails to disclose useful structures and conductive filler structure formed on a plane.

Hirakawa does not disclose such an integrated circuit arrangement. Figure 4 illustrates two structures which might be regarded as filler structures. The first filler structure 104-2 is provided on the left side on an oxide layer portion having increased oxide thickness compared to gate oxide under gate electrode 104-1. This filler structure 104-2, however, is part of a wordline as disclosed in column 4, line 62 and accordingly performs an electrical circuit-oriented function. Furthermore, this structure cannot be regarded as a filler structure because this elevated structure does not fill recesses on the thinner gate oxide in the center portion of Figure 4.

The other conductive filler structure on the right side of Figure 4 (without reference number) also has an electrical circuit-oriented function because it contacts the right source/drain implantation region of the transistor

being formed with gate electrode 104-1. The contact structure for the left source/drain-implantation region is not illustrated; it seems to be provided above or below the drawing plane illustrating the cross-section of Figure 4. However, because of its electrical circuit-oriented function, the right conductive structure without reference number is an electrode contact structure rather than a dummy filler structure.

Furthermore, even if, for the sake of argument, it were to be construed as a filler structure, it would be deposited on a gate oxide layer. Figure 4 however illustrates that the gate oxide layer extends below gate electrode 104-1 but above the structure having no reference number; accordingly the right "dummy filler structure" has not been formed from the same patterned layer as the useful (gate) structure.

Appellants assert that the feature (in the second method step) that the conductive useful structures and the conductive filler structure are both formed by applying and structuring a conductive layer must inherently mean applying and structuring one and the same conductive layer (by referencing "*a* conductive layer"). This implicitly includes the feature that these kinds of structures have the same height.

Hirakawa fails to disclose that both the useful structure 104-1 and the "dummy filler structure" on the right side of Figure 4 (without reference number) are formed by applying and patterning one and the same conductive layer.

For these reasons, Appellants assert that the claim language clearly distinguishes over the prior art, and respectfully request that the Board

reverse the Examiner with respect to the 35 U.S.C. §102 rejections.

Argument 4—New Matter and Written Description Rejections of Claims 22 and 24

(These issues are discussed together because of their interrelatedness)

Examiner's Position: Claims 22 and 24 recite a limitation relating to conductive filler structures arranged to establish a uniform geometrical occupation by the conductive useful structures and the conductive filler structures. This language constitutes the introduction of new matter and is not supported by the original disclosure.

In the Office Action, on pages 2, the Examiner states:

> The amendment filed on September 15, 2003 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:
>
> Claim 22 recites the limitation "a plurality of conductive filler that are arranged to establish a uniform geometrical occupation by the conductive useful structures and the conductive filler structures" in lines 3-5. However, the recited limitation does not have a support as the specification originally filed. Applicants are required to cancel the new matter in the reply to this Office Action.
>
> Claim 24 recites the limitation "the conductive filler structures being arranged such that a uniform geometrical occupation by the conductive useful structures and the conductive filler structures is established" in lines 2-4. However, the recited limitation does not have a support as the specification originally filed. Applicants are required to cancel the new matter in the reply to this Office Action.

The Examiner further states, on pages 2-3 in rejecting these claims under 35 U.S.C. §112, first paragraph:

> Claims 22 and 24 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably

convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 22 recites the limitation "a plurality of conductive filler that are arranged to establish a uniform geometrical occupation by the conductive useful structures and the conductive filler structures" in lines 3-5. However, the recited limitation does not have a support as the specification originally filed. Therefore, the claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 24 recites the limitation" the conductive filler structures being arranged such that a uniform geometrical occupation by the conductive useful structures and the conductive filler structures is established" in lines 2-4. However, the recited limitation does not have a support as the specification originally filed. Therefore, the claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Appellants' Position: Support for the added claims 22, 24 can be found in the Specification, as originally filed.

Supporting language for dependent claim 22 can be found in the originally filed application on page 6, lines 11 to 13. Claim 24 corresponds to claim 22 and depends on independent method claim 18.

This portion of the Specification states:

They [conductive filler structures 72] are arranged such that a uniform geometrical occupation by the conductive useful structures and the conductive filler structures is established.

This aspect is illustrated by the embodiment shown in Fig. 3 and described in the preceding portion of the paragraph containing this sentence.

The Examiner fails to indicate how the language used in the originally

disclosed specification differs from that in the newly added claims.

For these reasons, Appellants assert that the claim language clearly distinguishes over the prior art, and respectfully request that the Board reverse the Examiner with respect to the 35 U.S.C. §§112 and 132 rejection.

CONCLUSION:

For the above reasons, Appellants respectfully submit that the Examiner is in error in law and in fact in rejecting claims 11, 12, and 15-24 based on the teachings of the above-discussed references. Reversal of the rejection of all of those claims is justified, and the same is respectfully requested.

Appellants are enclosing a check for the present appeal brief fee of $330.00 due as required by 37 C.F.R. §1.17(c). The Commissioner is hereby authorized to charge any additional fee that may be required to deposit account No. 50-1519.

Respectfully submitted,

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APPENDIX A
CLAIMS INVOLVED IN THE APPEAL

Claims 1-10 (previously cancelled).

11. (currently amended) An integrated circuit arrangement comprising:

a semiconductor substrate having at least one doped region; ~~and~~

a plane arranged on a surface of said semiconductor substrate and having a number of conductive useful structures and at least one conductive filler structure which exhibits essentially the same height, said conductive filler structure having no circuit-oriented function, said conductive filler structure being conductively connected to said doped region; and

a contact connecting said conductive filler structure to said doped region via a through hole;

wherein said through hole overlaps said conductive filler structure and said doped region exposing a surface of said conductive filler structure and a surface of said doped region, said contact being in communication with said surface of said conductive filler structure and said surface of said doped region.

12. (previously presented) The integrated circuit arrangement according to claim 11, further comprising:

a planarizing insulation layer surrounding said conductive useful structures and said conductive filler structure; and

wherein said conductive useful structures and said conductive filler structure are essentially a same height.

13-14. (currently cancelled)

15. (previously presented) The integrated circuit arrangement according to claim 11, wherein said conductive useful structures are gate electrodes; and wherein said conductive filler structure contains a material of said gate electrodes.

16. (previously presented) The integrated circuit arrangement according to claim 11, wherein said doped region is a doped well in said semiconductor substrate.

17. (previously presented) The integrated circuit arrangement according to claim 11, further comprising:

a metallization layer arranged above said plane wherein said conductive filler structure is arranged; and

a further contact connecting said conductive filler structure to said metallization layer.

18. (previously presented) A method for manufacturing an integrated circuit arrangement, said method comprising the steps of:

forming a doped region in a semiconductor substrate;

forming a plane on a surface of said semiconductor substrate by applying and structuring a conductive layer, said plane having a number of conductive useful structures and at least one conductive filler structure;

producing an insulation layer surrounding and covering said conductive useful structures and said conductive filler structure; and

producing a conductive connection between said conductive filler structure and said doped region.

19. (previously presented) The method according to claim 18, wherein said step of producing a connection between said conductive filler structure and said doped region further comprises the steps of:

opening a through hole in said insulation layer, said through hole respectively partially overlapping said conductive filler structure and said doped region for partially uncovering a surface of said doped region and a surface of said conductive filler structure; and

forming a contact in said through hole, said contact being in communication with said surface of said conductive filler structure and said surface of said doped region.

20. (previously presented) The method according to claim 18, further comprising the steps of:

producing a metallization layer above said plane wherein said conductive filler structure is formed; and

producing a further contact connecting said conductive filler structure to said metallization layer.

21. (previously presented) The integrated circuit arrangement according to claim 11,

wherein said doped region is said semiconductor substrate.

22. (previously presented) The integrated circuit arrangement according to claim 11, wherein the at least one conductive filler structure comprises:

a plurality of conductive filler structures that are arranged to establish a uniform geometrical occupation by the conductive useful structures and the conductive filler structures.

23. (previously presented) The method according to claim 18, wherein the conductive useful structures and the conductive filler structure exhibit essentially the same height, the conductive filler structure having no circuit-oriented function.

24. (previously presented) The method according to claim 18, wherein a plurality of conductive filler structures is provided, the conductive filler structures being arranged such that a uniform geometrical occupation by the conductive useful structures and the conductive filler structures is established.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on July 13, 2004.